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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,333	02/09/2004	Hiroshi Okumura	Q77321	8920
23373	7590	03/09/2005	EXAMINER	
SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037				MONDT, JOHANNES P
		ART UNIT		PAPER NUMBER
		2826		

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/773,333	OKUMURA, HIROSHI	
	<b>Examiner</b>	<b>Art Unit</b>	
	Johannes P. Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 31 January 2005.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) 18-28 is/are withdrawn from consideration.
- 5) Claim(s) 11-17 is/are allowed.
- 6) Claim(s) 1-8 is/are rejected.
- 7) Claim(s) 9 and 10 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | Paper No(s)/Mail Date: _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>2/9/04</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

***Election/Restrictions***

1. Applicant's election without traverse of the Group I invention (claims 1-17) in the reply filed on January 31, 2005 is acknowledged.

***Information Disclosure Statement***

2. The examiner has considered the items listed in the Information Disclosure Statement filed February 9, 2004; however, only the English abstracts and the commentary in the Specification concerning the relevance of said IDS documents (only for "prior art" 1-3; see paragraphs [03]-[06]) are readable to the examiner as he has no knowledge of Japanese. A signed Form PTO/SB/08 has been enclosed with this office action.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. **Claims 1-3 and 4-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant in view of Yanai et al (US 2003/0025127 A1).  
Prior Art as Admitted by Applicant teaches:

a thin film transistor substrate (page 1, Description of the Prior Art" and Prior Art Figure 1) comprising:  
an insulating substrate 301 (see par. [03]);

a first thin film transistor (driver transistor with gate 304) formed above said insulating substrate (cf. Figure 1), wherein said first thin film transistor comprises a first active layer 302 (island-like portion to the left in Figure 1; see [03]) formed above said insulating substrate, a first gate insulating film 303 (see [03]) formed on said first active layer and a first gate electrode 304 (see [03]) formed on said first gate insulating film (cf. Figure 1); and

a second thin film transistor (pixel transistor with gate 307) formed above said insulating substrate (cf. Figure 1), wherein said second thin film transistor comprises a second active layer 302 (island-like portion of 302 to the right in Figure 1; see [03]) formed above said insulating substrate, and a second gate insulating film 303/306 (see [03]) formed on said second active layer, a second gate electrode 307 (see [03]) formed on said second gate insulating film,

wherein a thickness of said second gate insulating film 303/306 is larger than a thickness of said first gate insulating film 303, by the thickness of 306 (see [03]),

wherein said second active layer 302 has at least two impurity doping regions 305b (see [03]) which overlap said second gate electrode 307,

wherein said second gate electrode comprises a semiconductor layer (polysilicon layer; see [02]).

*Prior Art as Admitted by Applicant also teaches said first active layer has at least two impurity doping regions 305a, but does not necessarily teach the limitation that said at least two impurity doping regions are formed in a self-aligning manner with respect to said first gate electrode. However, it would have been obvious to include said limitation*

*in view of Yanai et al*, who teach for the specific purpose (see [0040]) of simplifying the manufacturing process in a semiconductor TFT device comprising both a low-voltage driven TFT region and a high-voltage driven TFT region, the impurity regions of the low-voltage driven TFT can be formed in self-alignment (see abstract, and [0040], [0148]-[0150], Figure 4A).

*Furthermore, although met by Yanai et al as discussed above, the limitation "formed in a self-aligning manner with respect to said gate electrode" only has patentable weight in the result for the final structure. In reference to the claim language referring to "formed in a self-aligning manner with respect to said gate electrode" intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).*

*On claim 2: said second gate insulating film comprises said first gate insulating film 303 and a gate cover film 306 above said first gate insulating film (see [03]).*

*On claim 3: the limitation as defined by claim 3 is not necessarily taught by either the Prior Art as Admitted by Applicant, nor by Yanai et al. However, Yanai et al do teach said at least two impurity doping regions of the first active layer to be formed by self-aligning with a thickness of the first gate insulating film that is 30 nm (see Abstract), - which is a fraction of the claimed overlap of 100 nm (=0.1  $\mu$ m), in this context teaching that the LDD region portion 120 ([0152], [0160]) of one of said at least two impurity*

doping regions in one of two low-voltage TFTs (namely, the n-type TFT in a CMOS driver (consisting of a n-type TFT and a p-type TFT) (i.e., low in comparison to a pixel TFT; see Abstract, final sentence)) is located “just below” a drain-side edge of the gate electrode (see [0152]). Any overlap is thus seen to be of the order of or less than 30 nm. Applicant, in the Specification, does not explain why the difference between the gate-drain overlap between the gate and an LDD region formed by self-alignment just below a 30 nm thick gate insulating film and the claimed overlap 100nm or less is critical to his invention. Applicant’s disclosure does not teach why the difference between the range implicit in the prior art as cited here and the range as claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

*On claim 4:* at least one of said impurity doping regions formed in a self-aligning manner with respect to said first gate electrode includes an LDD structure 120 ([0152] and [0160]).

*On claim 6:* at least one of said impurity doping regions which overlap said second gate electrode includes an LDD structure (Abstract, final sentence).

5. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant and Yanai et al as applied to claim 1 above, and further in view of Oh (5,610,082). As *detailed above*, *claim 1 is unpatentable* over Prior Art as Admitted by Applicant in view of Yanai et al. *Neither necessarily teach* the further

limitation as defined by claim 5. *However, it would have been obvious to include said further limitation in view of Oh, who teach a gate-drain overlap of a switching TFT (Figure 3 and Background of the Invention, particularly col. 3, l. 8-27) that it is preferable to have a gate-drain overlap of between 1 – 2 µm. Motivation to include the teaching by Oh in the invention by the Prior Art as Admitted by Applicant is the consideration by Oh that parasitic capacitance limits the desirable overlap to below 2 µm (loc.cit.). Furthermore, Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).*

6. **Claims 7-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant and Yanai et al as applied to claim 1 above, and further in view of Okumura (JP 11307777 A) (IDS). *As detailed above, claim 1 is unpatentable over the Prior Art as Admitted by Applicant in view of Yanai et al. Neither Prior Art as Admitted by Applicant nor Yanai et al necessarily teach the further limitation as defined by claim 7. However, it would have been obvious to include said further limitation in view of Okumura, who in a patent document on TFTs for liquid crystal displays, hence closely related art and a/o including both low- and high- voltage transistors (namely: driver transistors (claim 7) and pixel transistors (claim 8), respectively), teaches the gate electrode to comprise a semiconductor layer 5 and a metal layer 6 (cf. Abstract) for the purpose of achieving high reliability and low cost (cf. Abstract). Motivation to include the*

teaching by Okumura in the invention at least derives from the stated high reliability and the lower resistance in comparison to a single polysilicon gate as taught by the Prior Art as Admitted by Applicant. *Combination* is easily achieved by adding to the polysilicon gate a metal film.

#### ***Allowable Subject Matter***

7. ***Claims 11-17*** are allowed. The following is a statement of reasons for the indication of allowable subject matter: while a separate gate electrode in a TFT on the opposite side of the active layer is well known in the art [see, e.g., Segawa et al (US 2002/0195604 A1): said gate electrodes 11 and 70 being on opposite sides of active layer 13c], strictly within the context of the limitation consisting of lines 1-16 of claim 11 a thin film transistor substrate wherein said second thin film transistor further comprises a third gate electrode between said second active layer and said second gate electrode, i.e., on the same side of said second active layer as said second gate electrode, has not been found in the prior art.

8. ***Claim 9*** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: while a separate gate electrode in a TFT on the opposite side of the active layer is well known in the art [see, e.g., Segawa et al (US 2002/0195604 A1): said gate electrodes 11 and 70 being on opposite sides of active layer 13c], strictly within the context of the invention of claim 1 a thin film transistor

substrate wherein said second thin film transistor further comprises a third gate electrode between said second active layer and said second gate electrode, i.e., on the same side of said second active layer as said second gate electrode, has not been found in the prior art.

9. **Claim 10** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: while a separate gate electrode in a TFT on the opposite side of the active layer is well known in the art [see, e.g., Segawa et al (US 2002/0195604 A1): said gate electrodes 11 and 70 being on opposite sides of active layer 13c], strictly within the context of the invention defined by claim 2 a thin film transistor substrate wherein said second thin film transistor further comprises a third gate electrode formed on said first insulating film, i.e., on the same side of said first active layer as said first gate electrode, has not been found in the prior art.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM  
March 6, 2005

Patent Examiner:



Johannes Mondt (Art Unit: 2826).